IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

YONEMARU — Atty. Ref.: 829-618

Serial No. 10/720,764 — TC/A.U.: 2826

Filed: November 25, 2003 — Examiner: DICKEY, T.

For: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS CONNECTED IN SERIES

* *

December 26, 2007

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Appellant hereby appeals to the Board of Patent Appeals and Interferences from the last decision of the Examiner.

TABLE OF CONTENTS

(I) REAL PARTY IN INTEREST

The real party in interest is Sharp Kabushiki Kaisha, a corporation of the country of Japan.

(II) RELATED APPEALS AND INTERFERENCES

The appellant, the undersigned, and the assignee are not aware of any related appeals, interferences, or judicial proceedings (past or present), which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

(III) STATUS OF CLAIMS

Claims 1, 6 and 8 are pending and have been rejected. Claims 2, 3, 5, 7 and 9-23 have been withdrawn from consideration. No claims have been substantively allowed. Thus, claims 1, 6 and 8 are on appeal herein, and claims 2, 3, 5, 7 and 9-23 are withdrawn from consideration.

(IV) STATUS OF AMENDMENTS

No amendments have been filed since the date of the Final Rejection.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

This section is for purposes of example only and is not limiting as to the claims.

The invention of the claims relates to a semiconductor integrated circuit (e.g., pg. 14, lines 14-15). The semiconductor integrated circuit includes one or more first cells (e.g., see S1 in Fig. 4; pg. 14, lines 15-16) that function(s) as a logic operation circuit (e.g., see 2 in Fig. 4; pg. 15, lines 13-15) for outputting data. The semiconductor integrated circuit further includes one or more second cells (e.g., see S2 in Fig. 4; pg. 14, lines 16-19) that function(s) as a driver circuit (e.g., see 1a-1e in Fig. 4; pg. 15, lines 15-18; pg. 40, lines 5-19) for driving the logic operation circuit (e.g., see 2 in Fig. 4) and a data retaining circuit (e.g., see 3 in Fig. 4; pg. 15, lines 16-18; pg. 49, lines 4-5) for retaining data output by the logic operation circuit (e.g., see 2 in Fig. 4). Each second cell (e.g., S2 in Fig. 1B) includes a PMOS transistor section and an NMOS transistor section (e.g., pg. 14, lines 18-20), the PMOS section (e.g., M05 in Fig. 1B, 2B) including a first PMOS transistor and a second PMOS transistor connected to the first PMOS transistor in series (e.g., see M05a, M05b in Figs. 1B, 2B; pg. 40, lines 5-18), the NMOS transistor section (e.g., M06 in Fig. 1B, 2B) comprising a first NMOS transistor and a second NMOS transistor connected to the first NMOS transistor in series (e.g., see M06a, M06b in Figs. 1B, 2B; pg. 40, lines 5-18). The first PMOS transistor and the second PMOS transistor are connected directly in series, and/or the first NMOS transistor and the second NMOS transistor are connected directly in series (e.g., pg. 40, lines 7-15). In certain example embodiments, a predetermined scheme is used to connect between the first cell and the second cell, between the plurality of transistors in the first cell, and between the PMOS transistor section and the NMOS transistor section in the second cell

(e.g., pg. 14, line 23 to pg. 15, line 3; pg. 42, lines 16-25; pg. 92, line 20 to pg. 93, line 16).

In certain example embodiments, a first second cell functions as the driving circuit part, and another second cell(s) functions as the data retaining circuit (e.g., see pg. 49, lines 4-5). In certain example embodiments of the claimed invention, multiple second cells are required for the driver and the data retaining circuit, respectively (e.g., pg. 40, lines 5-19; pg. 49, lines 4-5). In this respect, a plurality of second cells are provided and each of the second cells comprises the PMOS and NMOS characteristics recited in claim 1, and at least a first one of the second cells functions as a driver circuit for driving the logic operation circuit and at least a second one of the second cells functions as a data retaining circuit for retaining data output by the logic operation circuit (e.g., see pg. 49, lines 4-5 of the instant specification).

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First, whether claims 1 and 8 are anticipated under 35 U.S.C. Section 102(e) by Robinson (US 2005/0182809).

Second, whether claim 6 is unpatentable under 35 U.S.C. Section 103(a) over Robinson in view of Murakami (US 5,457,723).

(VII) ARGUMENT

It is axiomatic that in order for a reference to anticipate a claim, it must disclose, teach or suggest each and every feature recited in the claim. See, e.g., *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983). The USPTO has the burden in this respect.

Moreover, the USPTO has the burden under 35 U.S.C. Section 103 of establishing a prima facie case of obviousness. *In re Piasecki*, 745, F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). It can satisfy this burden only by showing that some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would have led that individual to combine the relevant teachings of the references to arrive at the claimed invention. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Before the USPTO may combine the disclosures of the references in order to establish a prima facie case of obviousness, there must be some suggestion or rationale for doing so. *In re Jones*, 958 F.2d 347 (Fed. Cir. 1992). Prior art references can be combined to render an invention obvious only if there is some apparent reason, either in the references themselves or in the knowledge generally available to one skilled in the art, to combine them. *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 82 USPQ2d 1385 (2007). Even assuming, *arguendo*, that a given combination of references is proper, the combination of references must in any event disclose the features of the claimed invention in order to render it obvious.

Furthermore, with respect to the inherency rejections, the law is clear that for something to be "inherent" in a reference, it must "necessarily" be present. *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The fact that

a certain result or characteristic "may" occur or be present in the prior art is not sufficient to establish the inherence of that result of characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). The Board of Appeals has made clear that "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

(i) Whether claims 1 and 8 are anticipated by Robinson under 35 U.S.C. Section 102(e)

Claim 1 stands rejected under Section 102(e) as being allegedly anticipated by Robinson (US 2005/0182809). This Section 102(e) rejection should be reversed for at least the following reasons.

Claim 1 requires that "*the first cell functions as a logic operation circuit for outputting data, and the second cell functions as a driver circuit for driving the logic operation circuit and a data retaining circuit for retaining data output by the logic operation circuit*; and wherein the first PMOS transistor and the second PMOS transistor are connected directly in series, and/or the first NMOS transistor and the second NMOS transistor are connected directly in series."

Thus, for example, referring to Fig. 4 of the instant application the first cell (e.g., S1) functions as a logic operation circuit (e.g., 2) for outputting data, and the second cell (e.g., S2) functions as a driver circuit (e.g., 1a-1e) for driving the logic operation circuit (e.g., 2) and a data retaining circuit (e.g., 3) for retaining data output by the logic operation circuit (e.g., 2). In certain example embodiments, a first second cell functions

as the driving circuit part, and another second cell(s) functions as the data retaining circuit (e.g., see pg. 49, lines 4-5). In certain example embodiments of the claimed invention, multiple second cells are required for the driver and the data retaining circuit, respectively. In this respect, a plurality of second cells are provided and each of the second cells comprises the PMOS and NMOS characteristics recited in claim 1, and at least a first one of the second cells functions as a driver circuit for driving the logic operation circuit and at least a second one of the second cells functions as a data retaining circuit for retaining data output by the logic operation circuit (e.g., see pg. 49, lines 4-5 of the instant specification).

The Office Action contends that the first cell and second cell recited in claim 1 correspond to the barrel shifter 62 and the clocked inverter 66, respectively, in Robinson. In addition, the Office Action contends that the clocked inverter (alleged second cell) 66 functions as a driver circuit for driving the barrel shifter 62 and as a dynamic latch.

However, contrary to allegations in the Office Action, the clocked inverter 66 of Robinson does not function as a driver circuit for driving the barrel shifter 62. The clocked inverter 66 together with a second inverter 67 dynamically latch the output of the barrel shifter 62 (see [0050] of Robinson). See clocked inverter 66 in fig. 9 denoted with reference numeral 70. The clocked inverter 66, 70 receives the output of the barrel shifter 62 as an input IN. Thus, the clocked inverter does not drive the barrel shifter 62. It appears as if the final Office Action contends that the clocked inverter 66 is a driver circuit for driving the barrel shifter 62 because the clocked inverter 66 includes a pull-up transistor 79 and a feedback path exists. However, although a feedback path may be present, such feedback path is only between the output OUT and input IN of the clocked

inverter 66, 70. That is, there is no feedback path from the clocked inverter 66, 70 back to an input of the barrel shifter 62 in order to drive the barrel shifter. The pull-up transistor merely performs voltage level restoration at the output of the barrel shifter (see [0053] of Robinson). Accordingly, it will be appreciated that the clocked inverter 66 in Robinson does not function as a driver circuit for driving the barrel shifter 62. Thus, Robinson fails to disclose or suggest that "*the second cell functions as a driver circuit for driving the logic operation circuit and a data retaining circuit for retaining data output by the logic operation circuit*" as recited in claim 1.

In the Advisory Action dated September 28, 2007, in response to the applicant's argument that the clocked inverter 66 (alleged second cell) in Robinson does not function as a driver circuit for driving the barrel shifter 62 (i.e., alleged first cell), the Examiner states that the "Applicant provides ABSOLUTELY NO GUIDANCE AS TO THE MEANING OF THE TERM, "DRIVER CIRCUIT." Furthermore, the Examiner states in the Advisory Action that "drive" is defined in the 1992 edition Academic Press Dictionary of Science and Technology as "application of voltage or power signals to a system circuit, or device to cause it to perform its intended function". Based on said definition of "drive", the Examiner argues in the Advisory Action that "the feedback circuit in Robinson's second cell 66 applies a voltage to the pass transistors of first cell 62 to perform voltage level restoration. This voltage level restoration is allegedly a "driving" function because it causes these pass transistors to perform their intended function. Therefore, the Examiner argues that the feedback circuit is a "driver circuit" for first cell 62.

However, the Examiner's allegation is incorrect. Robinson discloses that "[when] pass transistors are used to implement the barrel shifter 62, high level output signals from the barrel shifter experience voltage degradation." In order to prevent such voltage degradation, the pull-up transistor 79 in the clock inverter 66 is used to perform voltage level restoration. Specifically, the voltage level restoration is performed by turning on the pull-up transistor 79 so that the input of the clock inverter 66 is coupled to the supply voltage Vdd, which supplies the desired high level voltage (see, e.g., paragraph [0053]). In other words, pull-up transistor 79 in the clock inverter 66 performs the function of preventing voltage degradation of the high level output signals from the barrel shifter 62 by restoring voltage level within the clocked inverter 66 itself, not in the barrel shifter 62.

Robinson fails to teach or suggest that the clocked inverter 66, 70 drives the barrel shifter 62. The dictionary definition of the term "drive" provided by the Examiner means the application of voltage or power signals to a system, circuit, or device to cause it to perform its intended function. However, the clocked inverter 66, 70 of Robinson does not apply voltage or power signals to barrel shifter 62 to cause the barrel shifter 62 to perform its intended function. Based on the definition of "drive" provided by the Examiner, in order for the clocked inverter 66 (i.e., alleged "second cell") to "drive" the barrel shifter 62 (i.e., alleged "first cell"), the clocked inverter 66 needs to apply a voltage or power signal to the barrel shifter 62 (i.e., "first cell") to cause it to perform its intended function. However, as discussed above, the clocked inverter 66 does not apply a signal to the barrel shifter 62 for causing the barrel shifter 62 to perform its intended function, since a signal from the clocked inverter 66 is not input into the barrel shifter 62. In contrast with claim 1, it is clear that the barrel shifter 62 outputs a signal to the clocked

inverter 66, 70 (see [0053] of Robinson – "when the input to the clocked inverter 70 goes to the degraded high level that is *output by the barrel shifter*"). Therefore, contrary to the Examiner's allegation, the clocked inverter ("second cell") 66 does not function as a driver circuit for driving the barrel shifter 62.

In addition, the Examiner alleges that on page 3 of the Remarks submitted by the Applicant in response to said Final Office Action, the Applicant admits that (a) the clocked inverter 66 provides a signal to the barrel shifter 62, and that (b) said signal is needed to provide voltage level restoration required for the proper functioning of the barrel shifter 62. Applicant disagrees with these allegations. Specifically, on page 3 of the Remarks, applicant stated that "there is no feedback path from the clocked inverter 66, 70 back to an input of the barrel shifter 62 in order to drive the barrel shifter." In other words, applicant argued that the clocked inverter 66 does not provide a signal to the barrel shifter 62. Since applicant argued the non-existence of the signal, (b) certainly was not admitted in any respect.

For at least the foregoing reasons, the anticipation rejection of claim 1 should be reversed.

Claim 8 is dependent on claim 1, and is in condition for allowance at least because the claim from which it depends (claim 1) is in condition for allowance.

(ii) Whether claim 6 is unpatentable over Robinson in view of Murakami under 35 U.S.C. Section 103

Claim 6 is dependent on claim 1, and is in condition for allowance at least because the claim from which it depends (claim 1) is in condition for allowance. However, it is noted that applicant does not agree with the combination used to reject claim 6 as well.

CONCLUSION

In conclusion it is believed that the application is in clear condition for allowance; therefore, early reversal of the Final Rejection and passage of the subject application to issue are earnestly solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Joseph A. Rhoa
Reg. No. 37,515

JAR:caj
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

(VIII) CLAIMS APPENDIX

1. A semiconductor integrated circuit, comprising:

a first cell comprising a plurality of transistors;

a second cell comprising a PMOS transistor section and an NMOS transistor section, the PMOS transistor section comprising a first PMOS transistor and a second PMOS transistor connected to the first PMOS transistor in series, the NMOS transistor section comprising a first NMOS transistor and a second NMOS transistor connected to the first NMOS transistor in series,

wherein a predetermined scheme is used to connect between the first cell and the second cell, between the plurality of transistors in the first cell, and between the PMOS transistor section and the NMOS transistor section in the second cell,

the first cell functions as a logic operation circuit for outputting data, and the second cell functions as a driver circuit for driving the logic operation circuit and a data retaining circuit for retaining data output by the logic operation circuit; and

wherein the first PMOS transistor and the second PMOS transistor are connected directly in series, and/or the first NMOS transistor and the second NMOS transistor are connected directly in series.

6. A semiconductor integrated circuit according to claim 1, wherein the plurality of transistors in the first cell include a PMOS transistor and an NMOS transistor.

8. A semiconductor integrated circuit according to claim 1, wherein:

the first PMOS transistor, the second PMOS transistor, the first NMOS transistor, and the second NMOS transistor each comprise a gate, a source, and a drain;

a first source voltage is applied to the source of the first PMOS transistor;

a second source voltage is applied to the source of the first NMOS transistor;

one of the gate of the first PMOS transistor and the gate of the second PMOS transistor is connected to an input terminal, an input signal being input to the input terminal, and the other is connected to a first gate control signal input terminal, a first gate control signal being input to the first gate control signal input terminal;

one of the gate of the first NMOS transistor and the gate of the second NMOS transistor is connected to the input terminal, and the other is connected to a second gate control signal input terminal, a second gate control signal being input to the second gate control signal input terminal; and

the drain of the second PMOS transistor and the drain of the second NMOS transistor are connected to an output terminal.

(IX) EVIDENCE APPENDIX

None

(X) RELATED PROCEEDINGS APPENDIX

None